

Preliminary Datasheet SL2002: Integrated Laser Driver

Features

- Flexible architecture can provide laser FWHM pulses less than 2ns
- High charging efficiency from a single 2.8V to 6V
- Peak Power 200W
- Integrates needed blocks for Charging and Firing Resonant-Mode Diode Lasers
- Inductor Current Control offers precise Resonant Capacitor Energy even with Input Voltage Fluctuations
- Up to 1 MHz Rep Rate limited by temperature rise in laser and other board components
- Minimal external components enable extremely integrated and efficient layout
- Integrated I2C interface for Output Power Control and Fault monitoring
- 1 mm x 3.5 mm WLCSP Package utilizing bumped die

Applications

- Laser TOF Measurement Systems
- LIDAR
- Range Finding
- 3D Mapping

Product Description

The SL2002 is an Integrated Timing Controller, Boost Voltage Generator, and Driver for Laser Time-of-Flight Measurement Systems employing Edge Emitting Laser Diodes or VCSEL Diodes.

This device provides the ease-of-design of a simple resonant flash TOF laser system but is integrated together with a boost charger and proprietary charge control to efficiently charge the resonant capacitor to the optimum voltage and a GANFET Driver to fire the laser.

The integrated Pulse Timing Controller uses a proprietary Architecture to provide Laser Diode pulses less than 3 ns wide and capable of providing 200 watts of Peak Light power. An External MOSFET or small GANFET provides the "Flash" signal to fire the laser.

Integrated drivers provide needed signal for driving GAN FETs or MOS FETs

The Resonant Capacitor is charged during each pulse cycle via an internal boost charger. This integrated charging architecture minimizes losses normally associated with transferring charge from standard High Voltage Supply Rails. The supply voltage for the charger can be as low as 3 volts and still achieve laser diode voltages of > 100 volts. No external Boost Regulator is required.

An I²C interface is provided for setting the amount of charge in the resonant capacitor to regulate light power. Fuse option to also adjust output power via charger input voltage.

Output power can be tightly regulated by the charging circuit. With this high level of integration, it is possible to achieve the highest light power with optimum efficiency.

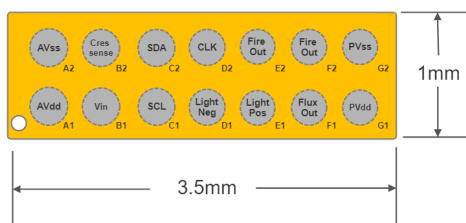


Figure 1: Top View SL2002

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Pin Out

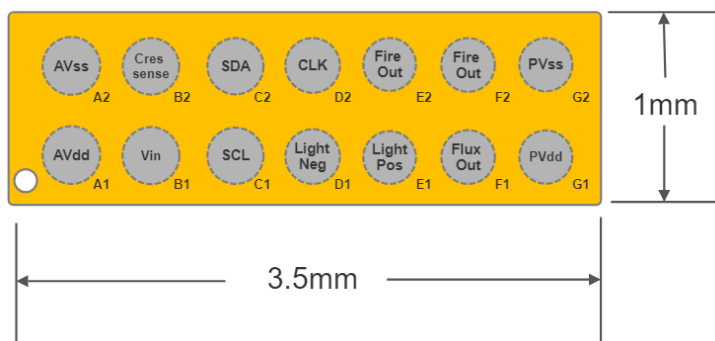


Figure 2: SL2002, 14 ball WCSP (0.5mm ball pitch) – Device Top View (bumps down)

Pin Definitions

Pin #	Name	Voltage Category (Vdc)	Description
A1	AVdd	LV: (5V)	Analog supply for inputs
A2	AVss	LV (0)	analog ground for inputs
B1	VIN	MV (24V)	inductor input voltage sense point
B2	Cres_SNS	LV (5V)	Cres voltage sense via external impedance
C1	SCL	LV (5V)	I ² C clock pin
C2	SDA	Output LV	I ² C data pin
D1	LIGHT NEG	Output LV	Output indicating Laser Firing. low on rising edge of FireOUT and stays low for 75ns or until FireOUT goes low
D2	CLK	LV (5V)	Dual function timing input for capacitor charge and laser firing (see Figure #)
E1	LIGHT POS	Output LV	Output indicating Laser Firing. high on rising edge of FireOUT and stays high for 75ns or until FireOUT goes low
E2	FireOUT	Output LV	Output Drive for MOSFET or EGaN FET for External Cathode Clamp
F1	FluxOUT	Output LV	Output Drive for MOSFET or EGaN FET for External Cathode Clamp
F2	FireOUT	Output LV	2 nd FireOUT pin (shorted to pin E2) for lower board impedance to FET gate
G1	PVdd	LV: (5V)	Power Supply for gate drive outputs
G2	PVss	LV (0)	Power Resonant Supply Voltage Rail Return for gate drive outputs

Table 1: SL2002 Pin Definitions

Commented [BR1]: Do we plan to keep the NC pins as NC for Tigerray? I was thinking that is just a hold-over from when we were planning to do a different die, but now it should be changed back to FireOUT and Light POS/NEG

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Functional Block Diagram

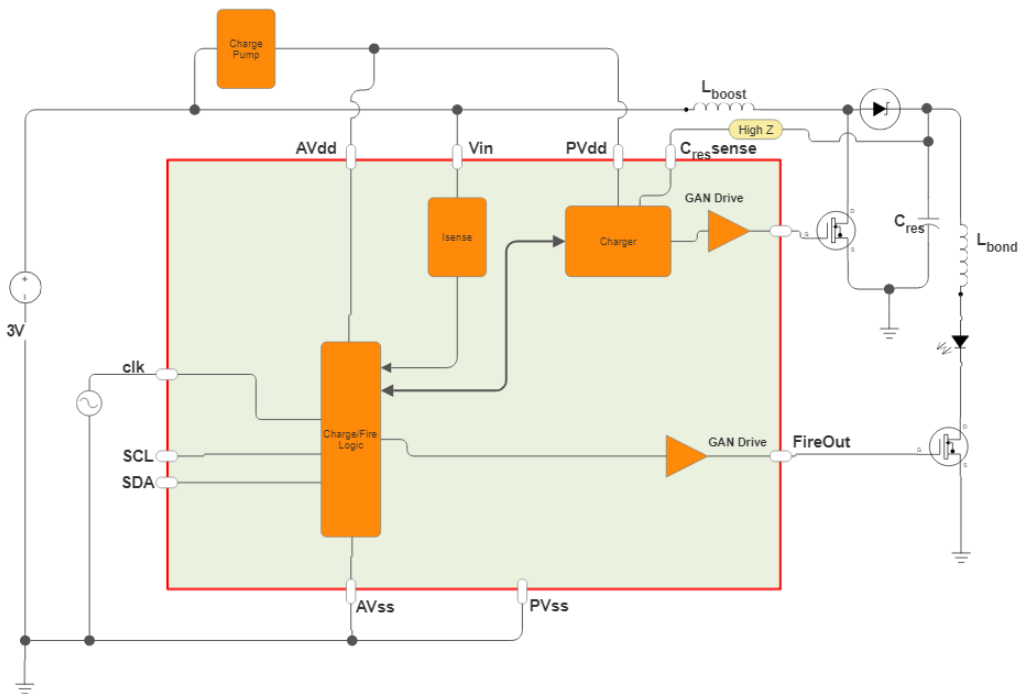
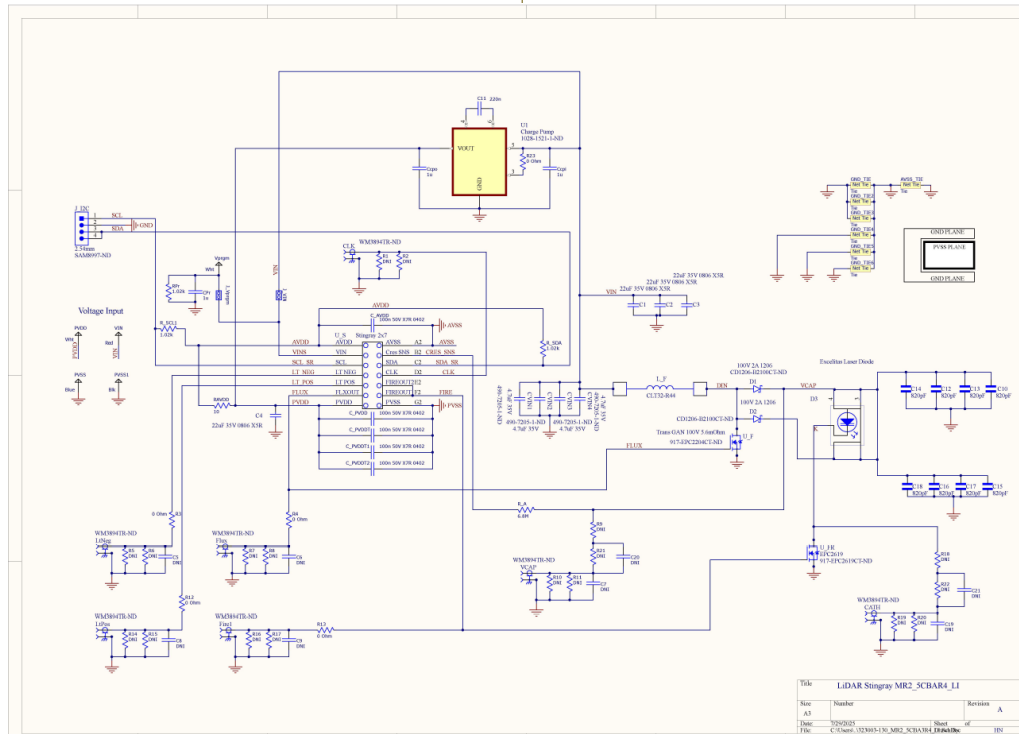


Figure 3: SL2002 Functional Block Diagram

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Typical Application Circuit



Commented [KB3]: Will be replaced with Stingray lite specific schematic with external charge pump

Commented [KB4]: To be replaced with charge pump board circuit

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Absolute Maximum Ratings Note 1

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Max.	Units
Pin Voltages - Inputs	CLK		-0.3	AVdd+0.3	V
	AVdd		-0.3	6.0	
	AVss		-0.3	0.3	
	Cf/PVdd		-0.3	6.5	
	PVss		-0.3	0.3	
	SCL, SDA		-0.3	AVdd+0.3	
	Cres_SNS		-0.3	AVdd+0.3	
Pin Voltages - Outputs	VIN		-0.3	6.5	V
	FireOUT		-0.3	6.5	
	FluxOut		-0.3	6.5	
Storage Temperature	T _{STG}		-50	150	°C
Junction Temperature	T _J		-40	150	
Lead Temperature ⁽³⁾	T _{LEAD}			260	
Electrostatic Discharge (ESD) Protection ⁽⁴⁾	V _{ESD}	HBM, Human Body Model per ANSI/ESDA/JEDEC JS-001	-2000	2000	V
		Charged-device model (CDM), per JEDEC specification	-500	500	V

Notes:

- 1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2) 1/16" from the case.
- 3) JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- 4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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Thermal Information Note 1

Parameter	Symbol	Typ.	Units
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	30	°C/W
Thermal Resistance Junction to Board	$R_{\theta JB}$	12	

Notes:

- 1) Simulated on 2S2P JEDEC 51-7 board.

Recommended Operating Conditions Note 1

(Ta = 25 °C Unless Otherwise Specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Vdd Supply Input Voltage	V_{Vdd}		4.5	5	6.0	V
VIN Voltage	V_{IN}		2.7		24	V
AVdd Bypass Capacitor	C_{AVdd}		0.1	-	10	μF
PVdd Bypass Capacitor	C_{PVdd}		0.1	-	10	μF
Vin Bypass Capacitor	C_{Vin}		10	-	-	μF
Operating Junction Temperature	T_J		-40		125	°C

Notes:

- 1) Device electrical characteristics are not guaranteed outside the recommended operating conditions.
- 2) Note that many electrical characteristics are specified for 4.5V < Vdd < 5.5V

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Electrical Characteristics

(Unless otherwise specified, 4.5V < AVDD < 5.5V, AVDD = PVDD, TJ = -40 °C to 125 °C recommended operating conditions.)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Supply Current (Vdd)						
Input Supply Current, No Load	I _{VDD(NL)}	Laser fire freq < 1kHz, DAC codes 150	-	1.0	-	mA
Input Supply Current, Pulsing	I _{VDD(SW)}	Laser fire freq = 250kHz?, Fire Out cap = 100pF ¹	-	3	-	mA
FireOut Drive Output – the two FireOut bumps are shorted on die						
FireOut Resistance Pull Down	V _{OL_FireOut}	I _{OL_FireOut} = 100mA			180	mΩ
FireOut Resistance Pull Up	V _{OH_FireOut}	I _{OH_FireOut} = 100mA			250	mΩ
Peak Sink Current	I _{OL_FireOut}	V _{OL_FireOut} = 5V ¹		12	-	A
Peak Source Current	I _{OH_FireOut}	V _{OH_FireOut} = 0V ¹		10		A
FluxOut Output						
FluxOut Resistance Pull Down	V _{OL_FluxOut}	I _{OL_FluxOut} = 100mA			720	mΩ
FluxOut Resistance Pull Up	V _{OH_FluxOut}	I _{OH_FluxOut} = 100mA			1	Ω
Peak Sink Current	I _{OL_FluxOut}	V _{OL_FluxOut} = 5V ¹		3	-	A
Peak Source Current	I _{OH_FluxOut}	V _{OH_FluxOut} = 0V ¹		2.5		A
FireOut Switching Parameters						
Maximum Switching Frequency ⁽¹⁾	f _{SW_MAX}	Note 1			10	MHz
Minimum On Time	T _{ON_MAX}	Minimum on time of the FireOut FET gate driver ¹	1			ns
Input Signal Parameters						
CresSNS resistance to AVss		While operating; forced to 0.2V		22		kΩ
CLK input rising threshold			1.7		2.6	V
CLK input falling threshold			1.1		1.8	V
CLK input voltage hysteresis			0.5		1	V
SDA/SCL input rising threshold					1.7	V
SDA/SCL input falling threshold			0.45			V
I ² C SCL Frequency					1	MHz
Timing Parameters						
CLK high to FluxOUT		CLK >50% to FluxOUT > 50%		5		ns
FluxOUT PW range from FluxOUT>50% to FluxOUT<50%		typ values for range, see Basic Timing Description Section explanation ¹	5		2800	ns
FluxOUT PW Accuracy from FluxOUT>50% to FluxOUT<50%		DAC code h'A8 on Flux Time Reg 100pF on FluxOUT, VIN=5V	188	200	212	ns
FluxOUT PW jitter from FluxOUT>50% to FluxOUT<50%		DAC code h'A8 on Flux Time Reg 100pF on FluxOUT, VIN=5V ^{1,2}	-1		+1	%
CLK high to FluxOUT jitter from Clock>50% to FluxOUT>50%		DAC code h'A8 on Flux Time Reg cycle to cycle jitter; 100pF on FluxOUT ^{1,2}	-2.5		+2.5	ns
FluxOUT rise time		20% to 80% of PVdd 100pF on FluxOUT ^{1,2}		0.45		ns
FluxOUT fall time		80% to 20% of PVdd 100pF on FluxOUT ^{1,2}		0.45		ns
FluxOut Low to FireOut High range from FluxOUT<50% to FireOUT>50%		typ values for range, see Basic Timing Description Section explanation ¹	10		2800	ns

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Parameter	Symbol	Condition	Min	Typ	Max	Unit
FluxOUT Low to FireOUT High Accuracy from FluxOUT<50% to FireOUT>50%		DAC code h'A7 on Charge Time Reg 100pF on FluxOUT & FireOUT ³		200		ns
CLK low to FireOUT		CLK <50% to FireOUT > 50% ¹		20		ns
FireOUT PW range from FireOUT>50% to FireOUT<50%		typ values for range, see Basic Timing Description Section explanation ¹	1		320	ns
FireOUT PW Accuracy from FireOUT>50% to FireOUT<50%		Tj -40C to +65C, DAC code h'7C on Fire Time Reg, 100pF on FireOUT ¹	4.5	5	5.5	ns
		same conditions as above -40C<Tj<125C ¹	4	5	6	ns
FireOUT PW jitter from FireOUT>50% to FireOUT<50%		DAC code h'7C on Fire Time Reg 100pF on FireOUT ^{1,2}	-4		+4	%
CLK low to FireOUT jitter from Clk<50% to FireOUT>50%		DAC code h'7C on Fire Time Reg cycle to cycle jitter; 100pF on FireOUT ^{1,2}	-5		+5	ns
Supply Voltage Threshold and Fault Protection Parameters						
AVdd & PVdd rising threshold			4.2	4.35	4.5	V
AVdd & PVdd falling threshold			3.9	4.05	4.2	V
AVdd & PVdd Vth Hysteresis				0.24		V
delay from Vdd rising threshold to laser firing enabled					1	ms
Vin Over Voltage accuracy		Vin > 6.5V	6	6.5	7	V
Vin Under Voltage accuracy		Vin <2.5V	2.3	2.5	2.7	V
Thermal Shutdown (OTP)	TSD	Note 1		150		°C
Thermal Shutdown Hysteresis	THYS	Note 1		20		°C
Cres pre-Charge OV		Vcres > 20V		20		V
Cres post Charge OV		Vcres > 110V		110		V
Cres pre-charge UV		Vcres < Vin – 1.3V		Vin-1.3V		V
Cres post-charge UV		Vcres < 18V		18		V

Notes:

- 1) Guaranteed by design and characterization, not production tested
- 2) cycle to cycle jitter is specified for no change in any environmental conditions. It shows a Gaussian distribution with 3 sigma numbers specified as limits
- 3) Only valid for operating mode where CLK falling edge does NOT trigger the laser to fire.

Detailed Descriptions

Overview

The SL2002 is designed for achieving optimal Laser Diode Timing and Drive for very short output Pulses. The SL2002 is a fully integrated Resonant Mode Controller for Driving EEL or VCSEL Laser Diodes. The SL2002 provides a predetermined amount of charge to the laser resonant capacitor each cycle from a low input voltage allowing the resonant capacitor voltage to increase as a function of the amount of charge. It is possible to have high resonant capacitor voltage from a relatively low input voltage which allows the use of small capacitors matching the predicted parasitic inductance found in series with the laser diode. This effectively eliminates the need for a boost converter to provide the needed high resonant Capacitor Voltage. A series inductor is used to provide the current to charge the resonant Capacitor to the needed voltage for the Laser Diode resonant circuit. The stored energy in the resonant

Commented [BR5]: Hong and Bill changed to absolute numbers with a little more than +/-7.5% variation (to get round numbers)

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capacitor is then transferred to the Laser Diode during the "Firing" phase. The SL2002 monitors in input Voltage (V_{in}) and adjusts the amount of time the input inductor is "fluxing" to compensate for variations in V_{in} . Fault trigger levels can be set for V_{in} undervoltage and overvoltage. The SL2002 also monitors the voltage on the resonant capacitor (C_{res}) for under and over voltage conditions. These Fault trigger points are set via internal registers and programmed over the I²C interface.

Detailed Pin Descriptions

Pins A1: AV_{dd} and A2: AV_{ss}

AV_{ss} is the Main ground return for the analog circuitry and the LIGHT_OUT signals. This circuitry is supplied by AV_{dd} , a decoupling capacitor between AV_{dd} and AV_{ss} should be placed as close as possible to the IC. AV_{ss} should nominally be tied to board ground within a few millimetres of the SL2002 in a board location that is outside of the current path between the ground input to the board and the ground of the resonant capacitors. Special attention should be paid to preventing switching noise between AV_{ss} and the ground pins of the chip that is receiving the LIGHT_POS and LIGHT_NEG output signals.

Pins G1: PV_{dd} and G2: PV_{ss}

PV_{ss} is the main power ground return for the gate drive circuitry. The gate drive circuitry is supplied by PV_{dd} . A decoupling capacitor between PV_{dd} and PV_{ss} should be placed as close as possible to the IC. PV_{ss} should be tied to the power ground plane in a manner to minimize inductive voltage ringing between the GaN FET used for laser firing (1st priority) as well as minimize the inductive voltage ringing between the GaN FET used for inductor current ramp (2nd priority).

Pin B1: V_{in}

This pin is used to sense the inductor input voltage for Fault recognition as well as to maintain a constant inductor peak current. The V_{in} over voltage and under voltage Fault Thresholds are set via register 0X13.

Pin B2: C_{res_SNS}

The C_{res_SNS} pin is used to sense the high voltage across the resonant capacitor utilizing an external resistor as shown in *Figure 18: Cres Sense from the Anode Side*. Value options include 6.2M Ω or 6.8M Ω , with the fault threshold voltages varying per *Table 8*. Please ensure that the external resistor can support the maximum voltage on the C_{res} net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action SL2002 takes when a fault is detected is described in *Table 4: Fault Conditions*.

Pins C1: SCL and C2: SDA

These are Clock and Data pins for I²C interface. The I²C Interface is always accessible. Four selectable I²C addresses are available for the SL2002. These are selected by changing bits 1 & 0 in register address 0x16. These bits can be changed via an I²C command, in which case the address will change immediately such that all subsequent I²C communication will use the new address. The address bits can also be loaded into the 3-time programmable MTP such that the I²C address option will always be loaded at part start-up, explained in *Table 2*.

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Register 0x16 bit1 bit0	I ² C Address
00	0001001x
01	0101001x
10	1001001x
11	1101001x

Table 2: I²C Startup Addresses

Pins D1: LIGHTNEG and E1: LIGHTPOS

These pins provide an indication of the **FireOUT** signal going high with an extremely small amount of signal jitter from period to period (3 sigma jitter <100ps).

Pin D2: CLK

This multi-function pin supplies the main clock to the pulse timing generator. The rising and falling edges of the clock can be programmed to trigger the gate drive outputs in 3 different modes as described in the timing control section below in **Error! Reference source not found.**

Pins E2 and F2: FireOUT

These pins provide an extremely fast gate drive signal with adjustable pulse width between 0.5ns and 100ns for the GaN or MOS Gate Drive. Two adjacent pins are used to reduce the parasitic inductance on the die and on the board.

Pin F1: FluxOUT

This pin provides a fast gate drive signal with adjustable pulse width between 5ns and 1μs for the GaN FET that is used to ramp current in the inductor and charge the resonant capacitor.

Basic Timing Description

Timing Steps

- 1). CLK rising edge triggers FluxOUT to rise, starting the Flux time (inductor current ramp).
- 2). The Flux time "Tflux(ns)" is controlled by register 0x10 with 2.5% steps from 5ns to 2.8μs as shown in *Figure 8*.
- 3). The Charge time "Tcharge(ns)" is controlled by the pulse width of the CLK input pin.
- 4). At the falling edge of the CLK input pin, the FireOUT signal goes high to begin the Fire time.
- 5). The Fire time "Tfire(ns)" is controlled by register 0x12 with 2.5% steps from 1ns to 320ns.

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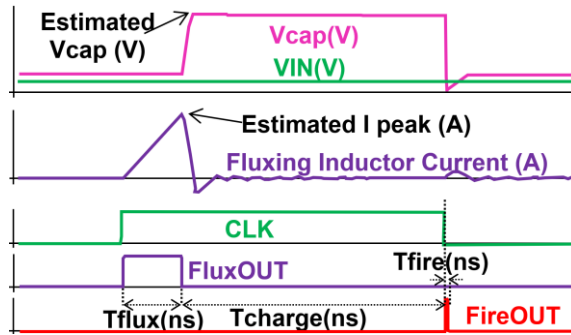


Figure 5: Mode 1 Timing Diagram

Timing Description

The timing for Fluxing, Charging (mode1 only) and Firing is controlled by the circuit in Figure 6 . A current (I1) is set-up by forcing a voltage (Vref1) across a DAC programmable resistance value. That current (I1) is then mirrored to a current I2 and used to charge a capacitance to a voltage level (Vref2). When the INPUT signal goes high, the PULSEout signal will go high until the capacitor is charged to the Vref2 level. The PULSEout high time will follow the equation:

$$\text{Equation 1: } PULSEout \text{ high} = \frac{C * Vref2 * Rdac}{Vref1 * Gmirror}$$

The PULSEout high time will change directly proportional to a change in the DAC resistance value (Rdac). The PULSEout high time will change inversely proportional to a change in the voltage of Vref1 or the gain of the current mirror (Gmirror).

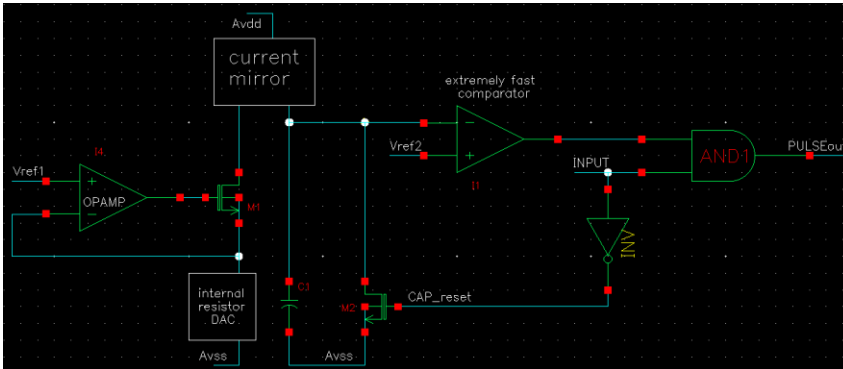


Figure 6: Timing and Firing Circuit

Three 8 bit registers (0x10h, 0x11h, 0x12h): FluxTime, ChargeTime and FireTime correspond to DACs for each of these timing parameters. Their resistor value increases by ~2.5% for each DAC step, with a minimum resistor value of 2kΩ and a maximum resistor value of 1.085MΩ with each resistor value set by the equation:

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Equation 2: $R_{dac\ value} = 2k * 1.025^{(R_{dac\ code})}$

for Rdac codes from zero to 255

Since the Rdac code is an exponent in the equation above, the Rdac value changes linearly on a log scale as shown in the graph in [Figure 7](#).

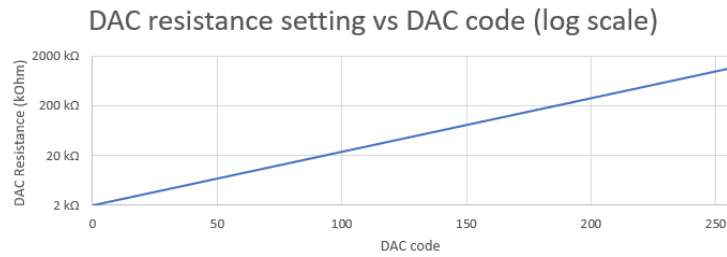


Figure 7: DAC Resistance vs. DAC Code

The equation for peak inductor current (I_{L_peak}) verses Flux time (T_{flux}) is:

Equation 3: $I_{L_peak} = V_{in} * \frac{T_{flux}}{L}$

The Flux time setting can be set to vary inversely proportional to the V_{in} voltage or to be fixed and not change as V_{in} changes. Per [Equation 3](#) above, when the Flux time is varied inversely proportional to the V_{in} voltage, a constant peak inductor current (I_{L_peak}) will be maintained.

The V_{in} dependent Flux time is set for an input voltage of 5V. For the 5V setting, the Flux time will automatically change inversely to V_{in} over a V_{in} range of 3.5V to 6.5V.

The graph below Figure 8 shows the inversely proportional behaviour of the Flux Time to the V_{in} voltage. The orange curve has longer Flux time due to the lower V_{in} voltages (3.5V for the 5V setting).

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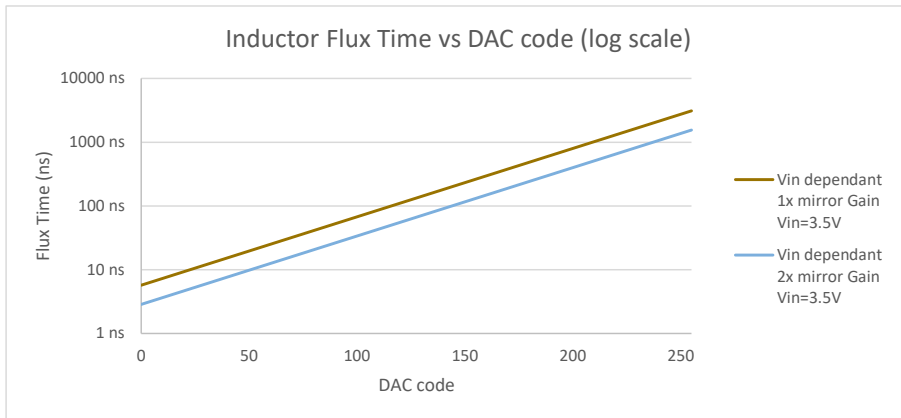


Figure 8: Inductor Flux Time vs. DAC Code

Since the Flux time is changing inversely proportional to the V_{in} voltage, the peak inductor current (I_{L_peak}) will be constant for a given value of inductance per [Equation 3](#).

The graph in [Figure 9](#) below shows the Tflux with Gmirror=1 & 440nH inductor or Gmirror=2 & 220nH inductor.

For smaller values of inductors, a 2x Gmirror setting is available. This mode almost doubles the current into the capacitor of [Error! Reference source not found.](#), which decreases the Flux Time for a given DAC setting by a factor of ~1.8.

Users can use the I²C interface to adaptively change the DAC resistor setting which varies the Inductor Flux time (Tflux). This will change the inductor peak current (I_{L_peak}) which in turn will increase or decrease the voltage of the resonant capacitor (C_{res}) and the current through the laser diode when it is fired. For customers who want to adaptively change the peak inductor current (I_{L_peak}), but do not want to use the I²C interface, an option is included where the part does not automatically vary the Flux time (Tflux) as V_{in} varies. With this option, the customer can vary V_{in} to change the inductor peak current (I_{L_peak}) according to [Equation 3](#)

The graph in

Figure 9: Inductor Flux Time vs. DAC Current

below shows the inductor flux time (Tflux) for the mode where the Flux time is independent of V_{in} for the 1x and 2x current mirror gain (Gmirror) settings.

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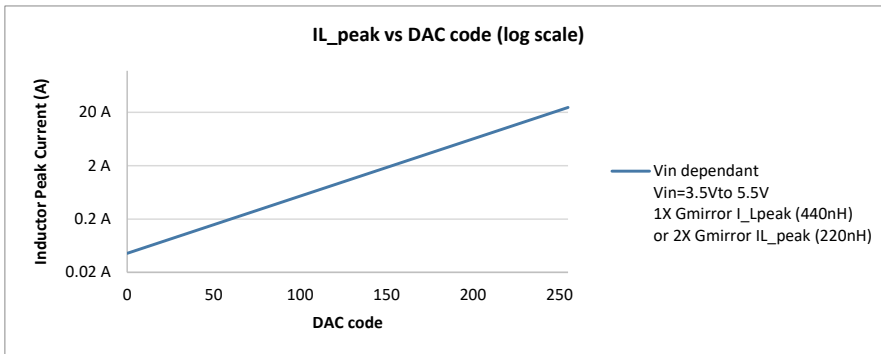


Figure 9: Inductor Flux Time vs. DAC Current

Since the Flux time is not changing as the V_{in} voltage changes, the peak inductor current (IL_{peak}) will change for a given value of inductance per [Equation 5](#) **Error! Reference source not found..**

The Graph in

[Figure 9](#): Inductor Flux Time vs. DAC Current

above shows the Flux Times at different values of V_{in} with a $G_{mirror}=1$ and a 440nH inductor or $G_{mirror}=2$ and a 220nH inductor.

Commented [KB6]: Will be redone for Vin Max 6V

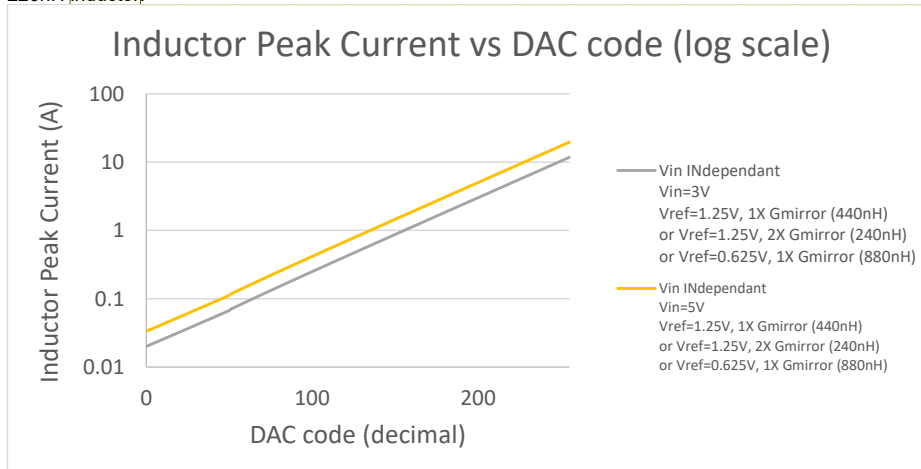


Figure 10: Peak Current vs. DAC Code

Per [Figure 11](#) below, the Schottky Anode Voltage is pulled to Ground during the Fluxing time such that the voltage across the inductor is fixed to $V_{in} - 0V = V_{in}$. Using the inductor Voltage to delta current equation, $V=L \cdot di/dt$, and knowing that the inductor current at the beginning of the Fluxing time is always zero, we can define the equation

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components as $V = V_{in}$, L =inductor value, i =current at the end of the Fluxing time, & dt =Fluxing time. By rearranging the equation, we can solve for the inductor current at the end of the Fluxing.

$$\text{Equation 4: } I_{Lpeak} = V_{in} * \frac{T_{flux}}{L}$$

$$\text{Equation 5: } I_{Lpeak} = T_{flux} * \frac{\sqrt{2}}{2 * L}$$

The default setting for the fluxing time control of the SL2002 uses the equation above to maintain a constant peak inductor current at the end of the Fluxing time (I_{L_peak}) by changing the Fluxing time inversely proportional to changes in the V_{in} voltage.

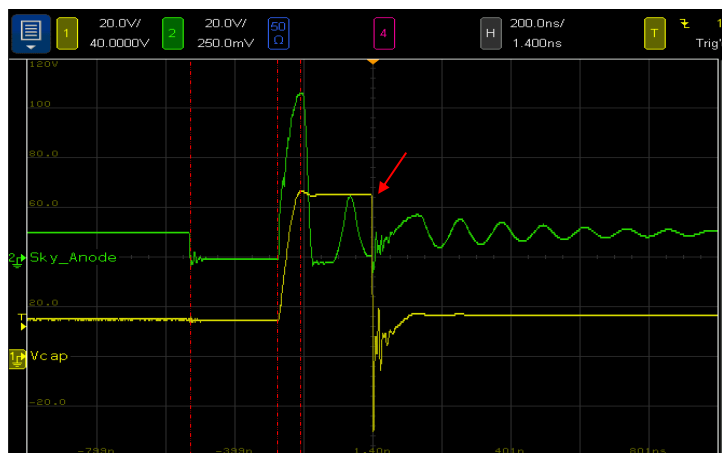


Figure 11: Charge and Firing

During the Charging time, the inductor current returns to zero as the resonant capacitor voltage is rising to a voltage above V_{in} . The charge applied to the resonant capacitor during this time is equal to $Q = I * \text{time}$, so a constant capacitor charge level can be maintained by changing current and charging time inversely proportional to each other. Since the peak current drops proportionally to changes in the inductor value, the Fluxing time will need to change by the square root of any change to the inductor value. For example, if the inductor value is doubled (2x) and the Fluxing time is increased by the square root of 2, then the inductor current at the end of the Fluxing time will change per the following equation:

but the charging time Δt will

increase per the following equation

$$\text{Equation 6. } \Delta t = \frac{I_{Lpeak}}{\sqrt{2}} * 2L$$

going back to the charge equation $Q = I * \text{time}$, we see that the charge will change by $1/\sqrt{2} * \text{time} * \sqrt{2} = 1$, so the charge supplied to the capacitor has not changed.

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Since the Fluxing time needs to increase by the square root of any increase in the inductor value to maintain a constant charge to the resonant capacitor, the user can input an inductor value range that the SL2002 will use to set the on-time. The inductor range settings do not need to match with the exact inductor value and they are simply used to modify the available range and step sizes for Fluxing time. The optional inductor range values are shown in [Table 3](#).

For proper operation of the adjustment for on-time versus V_{in} , the range is limited around 5V (3.0V to 6.0V).

The user can use the I²C and MTP address bits below to achieve 3 different fixed Flux time ranges per the table below:

decimal code	00x15 bit3=1 00x15 bit0=0	00x15 bit3=0 00x15 bit0=0	00x15 bit3=0 00x15 bit0=1
fixed Flux time range	low range	middle range	high range

Table 3: Inductor Range Selection: note that 00x15 bit 4 set to 1 for fixed Flux time Range selections

Based upon the Flux time range settings above, the user can program the peak current at the end of the Fluxing time per [Table 3](#).

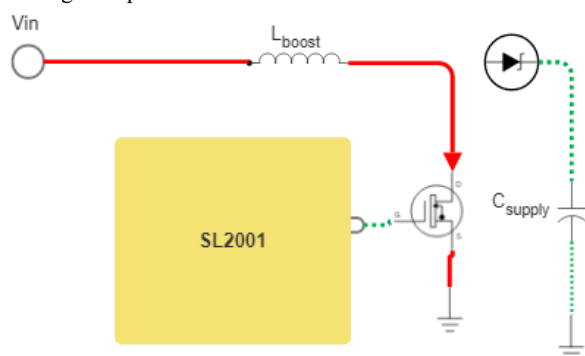


Figure 12: Inductor Flux Timing

For mode 2 described above, the Charge Time is set via the duty cycle of the clock.

The Charge Time should be set high enough to cover the post charge blanking times for the Cres sense overvoltage and undervoltage circuitry, which is ~400ns. 1μs is a good typical setting since it is not long enough to get any noticeable voltage degradation in the Cres voltage after charging while also covering the Cres sense blanking times with significant margin.

The Pulse Width of the FireOUT signal can be adjusted via register x12. This provides a balance between keeping the gate ON long enough to reach peak laser current and clamping the cathode voltage of the laser while at the same time turning OFF quickly enough to prevent a 2nd pulse of light through the laser. [Figure 13](#) below shows the Fire Time verses DAC code for the 3 possible DAC modes.

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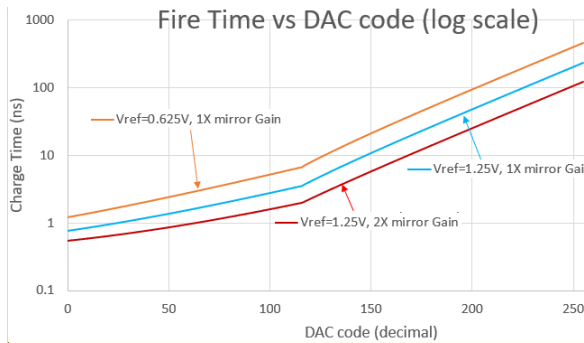


Figure 13: Fire Time versus DAC code

Commented [KB7]: Needs to be updated for 5V only

Protection and Fault information

The SL2002 offers several highly programmable fault options and settings. A brief summary of the Fault Options is shown below with more specific information regarding each option in the subsections below in [Table 4](#).

Hiccup Mode (Default): When a Fault is registered in the Digital circuitry, the SL2002 will stop immediately and set both the **FluxOUT** and **FireOUT** pins to low (zero V) for 28ms. After 28ms, the SL2002 will check whether the fault is still present. If the fault is still present, the SL2002 will continue holding both **FluxOUT** and **FireOUT** low and wait another 28ms before checking the fault status again. Once the fault is no longer present (checking every 28ms), the SL2002 will immediately begin driving both the **FluxOUT** and **FireOUT** pins again per the previous clock and timing settings.

Mask Faults: The SL2002 can be programmed via One Time Programmable ROM or via I²C to not shutdown or react to any of the faults desired.

Fault Latch Off mode: The SL2002 can be programmed via One Time Programmable ROM or via I²C to not “hiccup” but rather to “latch off” when any of the selected faults are registered. If the SL2002 does latch-off due to a fault, then the **FluxOUT** and **FireOUT** pins will be held low until either 1 of the 2 events occurs:

1. The DigSoftReset bit (bit 7 of register 0X15) is set to a 1 via the I²C interface (this bit will be reset back to 0 automatically upon reset)
2. The **AV_{dd}** voltage is brought below 1V, then brought back up above 3V

If either event 1 or 2 occurs, the SL2002 will go through its start-up sequence and all registers will be set according to the NVM settings. The SL2002 will then check for any faults before starting to drive the **FluxOUT** and **FireOUT** pins again.

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Fault Condition	Action
V _{DD} Low	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault Bit (Register 0x90 bit 0)
Cres Low After Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit1)
Cres High After Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit2)
Cres High Before Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit3)
Cres Low Before Cres Charge	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit4)
V _{in} Low	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit5)
V _{in} High	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit6)
Over Temperature	- Prevent FluxOUT and FireOUT pins from going high immediately - Trigger Fault bit (Register 0x90 bit7)

Table 4: Fault Conditions

Fault Behavior During Device Start-up

During start-up, approximately 100us after **AV_{dd}** has reached a voltage of ~2.5V, SL2002 will clear the reset for the internal Digital Engine. The **AV_{dd}** supply protection then activates. If the Digital Engine clears reset and **AV_{dd}** is still lower than 4.5V, a fault flag will be asserted to the Fault Register. During this initialization period the IC will not enter hiccup mode and waits for this fault to be cleared. Once **AV_{dd}** is above the target SupplyOK Fault rising threshold, the startup sequence will be completed, and functional mode will be enabled.

A SupplyOK fault will occur if the time for **AV_{dd}** to reach 4.5V from 2.5V is greater than 100μs. The slew rate can be determined by the equation below:

$$\text{Equation 7: } AV_{dd} \text{ Slew rate} > (4.5V - 2.5V)/100us = 2V/100us$$

Reading data from the OTP will take approximately 50us after the internal Digital Engine clears the reset state. The **V_{in}** Over Voltage and Under Voltage protection will be enabled with corresponding NVM pre-programmed thresholds. If a **V_{in}** UV or **V_{in}** OV fault exists when OTP read is complete, the corresponding fault bit will be asserted (Error! Reference source not found.). If the reported Fault is enabled, SL2002 will enter the shutdown mode with the corresponding pre-programmed shutdown state (Hiccup Mode or Latched Off).

To avoid the extra delay time during start up caused by a **V_{in}** UV Fault please note the following:

1. Ramp up the **V_{in}** supply to the target voltage before the **AV_{dd}** supply ramps or use the same supply for both **V_{in}** and **AV_{dd}** (Set **V_{in}** UV threshold to be 2.5V on the rising edge).
2. Ramp up **V_{in}** and **AV_{dd}** at the same time while keeping the **V_{in}** supply slew rate higher than the equation below:

$$\text{Equation 8: } V_{in} > UV_{\text{thresholdRising}} / (3V / \text{SlewRate_AV}_{dd} + 150\mu s + T_{\text{dlyprogramable}})$$

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The **CresSNS.UV_Precharge** comparator (see [Figure 17](#)) is active after OTP read is completed to detect a short circuit from the cathode of the laser to ground. The V_{in} voltage should not rise higher than the laser light threshold until at least 200us after the AV_{dd} voltage is higher than 2.5V for this start-up short detection to trip immediately during start-up (before the laser light causes an eye safety concern).

After all data from the OTP has been read, the device will wait a programmable amount of time (T_{dly} programmable) before the **FluxOUT** and **FireOUT** signals are enabled (allowed to go high), according to [Table 5](#).

bit5	bit4	Register 0x00, bits 5:4, FuseTime
0	0	Delay time from OTP read complete to Function mode allow is 18us
0	1	Delay time from OTP read complete to Function mode allow is 89us
1	0	Delay time from OTP read complete to Function mode allow is 355us
1	1	Delay time from OTP read complete to Function mode allow is 888us

Table 5: Programmable delays for OTP read mode to full Function mode.



Figure 14: Startup Waveforms where Vdd ramps slowly from the charge pump

Under a typical application setup, a charge pump can be used to convert low voltage V_{in} supply into 5V VDD for SL2002. When V_{in} supply is ramping up, V_{DD} will slowly follow and eventually reach the 5V target, see the waveform in [Figure 14](#) above. Depending on Charge Pump's output capability, V_{DD} might ramp up under different slew rates. When the slew rate is lower than 2V/100us, SL2002 IC will capture a supply fault during startup. However, this is only to gate the internal startup logic to prevent IC from starting operation with premature V_{DD} voltage. As soon as V_{DD} reaches 4.5V, the IC will enter full functional mode with a delay (assuming no other fault condition is occurring).

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Figure 15: Start-up waveforms for OTPready, FunctionMode and the CresSNS valid signal

During startup when OTP ready is completed, there is a programmable delay time before entering functional mode, see [Table 5](#) for options. In applications where Vin is below 4.5V, Cres UV pre-charge feature won't be enabled due to prevent fault mis-tripping.

During normal operation, the part reaction to a fault can be programmed. Register 0x01 (Fault Enable) individually sets each Fault such that it will cause an action, like the part shutting down. If the Fault Enable bit is not set (value of 0) for any individual fault and that fault type occurs, then the fault will be registered as a 1 in the status_fault register (0x90)

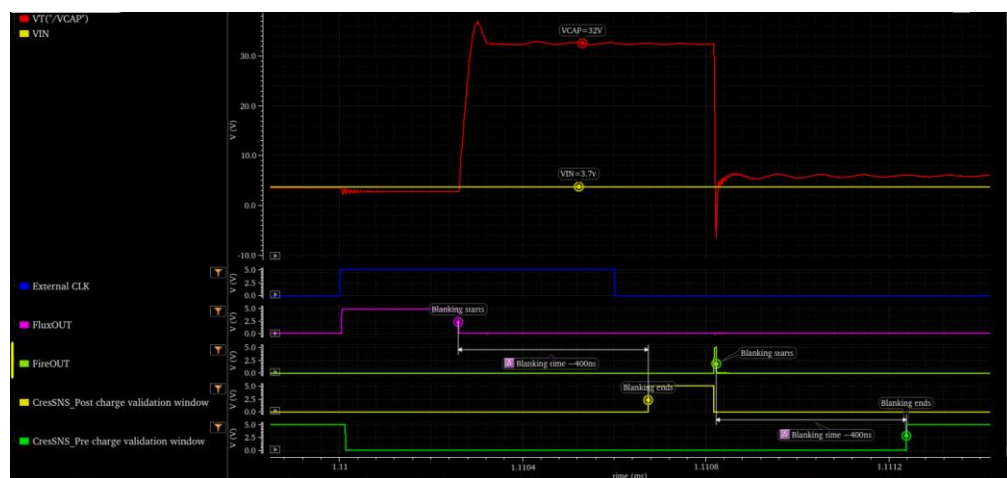


Figure 16: Fluxing and Firing Timing

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V_{in} UV and OV Faults

The Table below shows the Fault Threshold Options for V_{in} Undervoltage and Overvoltage Faults. If the V_{in} UV fault is disabled, the SL2002 will continue to operate even with V_{in} at zero. The undervoltage Faults are still Monitored to give an indication of V_{in} falling below the intended supply voltage range. The SL2002 V_{in} pin is rated for operation up to 5.5V; however, lower overvoltage threshold options are available for the user to get an indication of V_{in} going above their intended supply voltage range.

V _{in} UV Voltage Options	Register 0x13	
	Bit 1	Bit 0
2.5V	0	0
	NA	NA
	NA	NA
	NA	NA

Table 6: V_{in} UV Options

V _{in} OV Voltage Options	Register 0x13		
	Bit 5	Bit 4	Bit 3
	NA	NA	NA
	NA	NA	NA
	NA	NA	NA
	NA	NA	NA
	NA	NA	NA
	NA	NA	NA
6.5V	1	1	0
	NA	NA	NA

Table 7: V_{in} OV options

Cres Related Faults

The Cres_SNS pin is used to sense the high voltage across the resonant capacitor using an external resistor as shown in [Figure 17](#). Value options include 6.2MΩ or 6.8MΩ, with the fault threshold voltages varying per [Table 7: V_{in} OV options](#). Please ensure that the external resistor can support the maximum voltage that will be seen on the Cres net. The external resistor accuracy needs to be included in the accuracy of the OV and UV trip points. The action SL2002 takes when a fault as detected is described in [Table 5: Programmable delays for OTP read mode to full Function mode](#).

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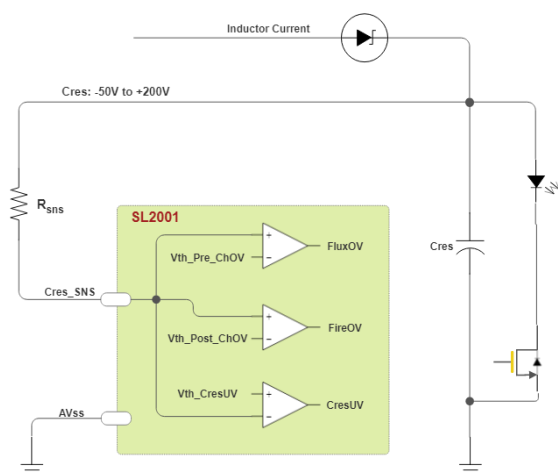


Figure 17: SL2002 Fault Diagram

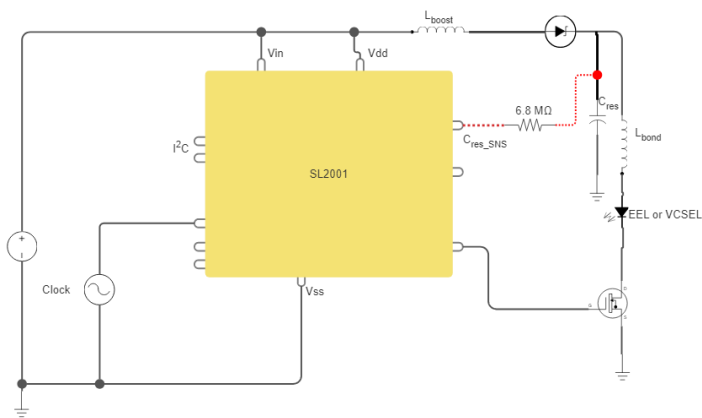


Figure 18: Cres Sense from the Anode Side



For example, in [Figure 18](#), when a weak short circuit occurs across the Laser firing GaN FET, it might only produce 100mA of current going through the Schottky diode. Therefore, the voltage drop across the Schottky diode isn't significant enough to be detected as a Cres UV pre-charge fault. This can cause the Laser diode to continue to emit light without being properly controlled. The Laser cathode sensing scheme ensures more accurate short circuit detection because of the additional voltage drop across the laser diode. It is recommended to add a resistor across the laser diode, 1K ohm as shown in [Figure 19](#). This enables the Laser cathode to settle faster and sync with the anode after the laser firing event, see [Figure 20](#). Here an example waveform is shown without any resistor between Laser Anode and Cathode. In this case the Cathode voltage doesn't reflect the true Anode (VCAP node) voltage before or after Laser fired. The resistor value should be chosen based on the value of parasitic capacitance in the Laser firing path (including Laser Firing GaN C_{ds} and PCB parasitic components), so that the 5*RC time constant to be <320ns. This ensures that the **CresSNS** input signal settles before the internal blanking time (for noise filtering) expires. When using 1K ohm RES across the laser, See [Figure 21](#), the Cathode voltage level will settle to the Anode voltage value after the RC delay time both before and after a Laser firing event.



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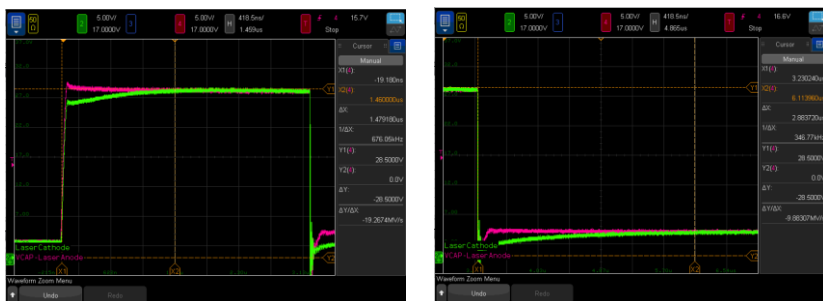


Figure 21: Laser Anode vs. Cathode with 1K ohm RES across Laser during operation

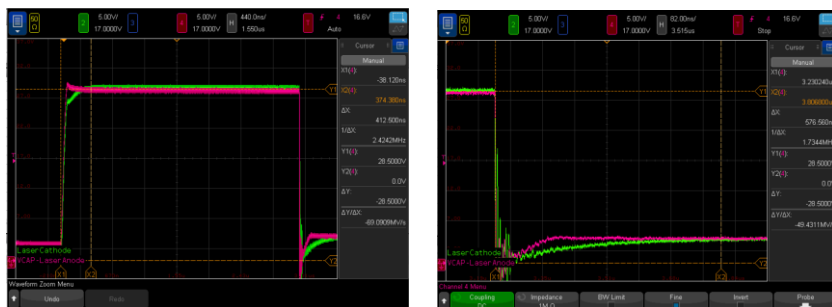


Figure 22: Laser Anode vs. Cathode with 180Ω resistor across Laser during operation

The SL2002 IC can capture a short circuit between Laser firing GaN FET source and drain. The reaction to this fault condition, can be programmed to force the SL2002 to turn on the Fluxing GaN FET which shunts current from V_{IN} to ground instead of going through the laser. This prevents the laser from emitting light until SL2002 IC goes through a power cycle or is digitally reset via I²C. *Figure 23* gives an example waveform using this cathode sensing scheme. In this example, the system starts up and encounters a short circuit between the Laser cathode and ground (source and drain of the Laser firing GaN FET). This protection scheme is only available when V_{IN} is above 4.5V to ensure accuracy and prevent mis-tripping. When the V_{IN} supply is ramping up, Laser diode will start to conduct current via the short circuit. Once the V_{IN} is above 4.5V, the short circuit is detected, and protection is activated. The **FluxOUT** pin will be latched to a high state to steer the current away from Laser to ground path.

Commented [KB8]: Looks like we cannot use this feature for Vin from a battery

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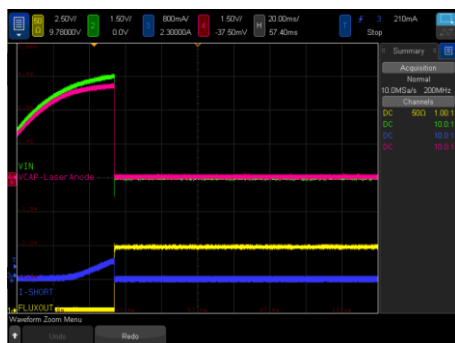


Figure 23: Laser firing GaN Short protection engaged after V_{DD} bias in place and during V_{IN} ramping up (cathode sense)

In applications where V_{DD} and V_{IN} supplies are combined the short circuit protection can still be triggered. However, because V_{DD} and V_{IN} are sharing the same supply, the Fluxing GaN will deplete V_{DD} and cause the IC to go into power on reset and turn off the Flux GaN FET. IF V_{IN} and V_{DD} try to rise again, a repeat of these events will occur if the short is still present. An input power fuse is recommended, to protect the system.

Commented [KB9]: This means that most likely the charge pump will go down and if set to hiccup mode, no eye safety

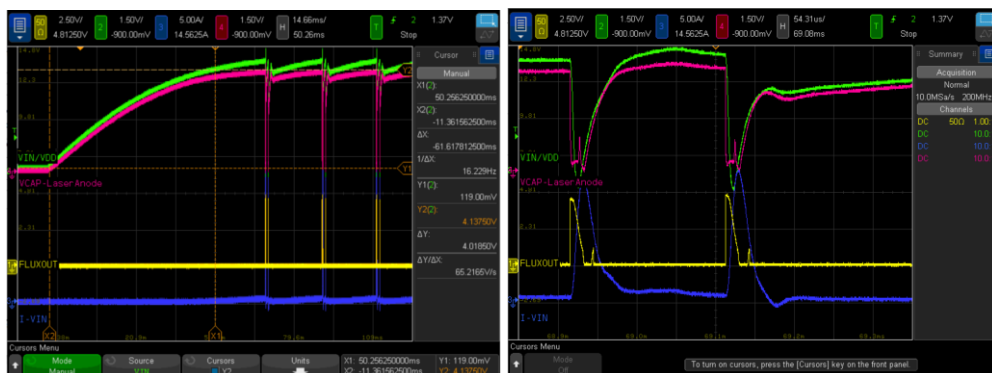


Figure 24: Laser firing GaN Short protection engaged when V_{IN} & V_{DD} are biased from the same supply and zoom in view (cathode sense)

During normal operation, a short circuit between the Laser cathode and ground can also be detected by the IC. An example of this occurrence is depicted in Figure 25. This short circuit occurs with a 1KHz repetition rate and is sensed using the laser cathode sensing scheme.

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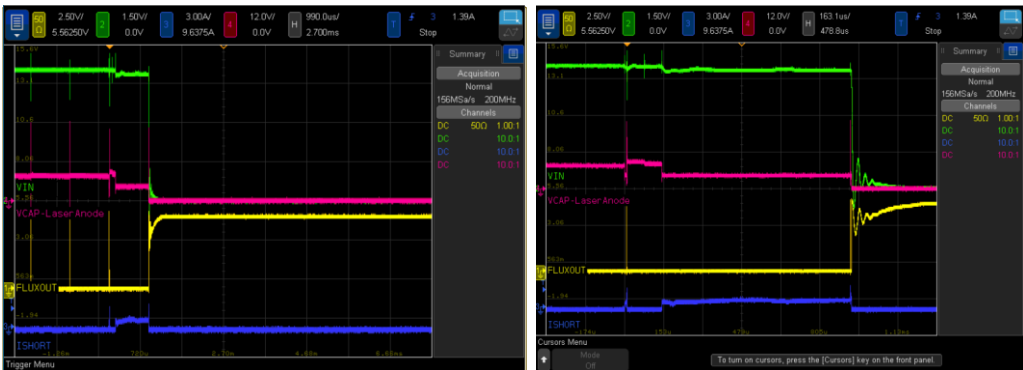


Figure 25: Laser firing GaN Short Circuit Protection engaged during operation when VIN & VDD are biased separately and zoomed in

Commented [KB10]: These graphs are not applicable for battery operation

Function	Cres Post Charge UV		Cres Post Charge OV		Cres Pre Charge UV		Cres Pre Charge OV	
Register	0x14, bits 4:2		0x16, bits 4:3		0x14, bits 1:0		0x14, bits 6:5	
Rsns value	6.2MΩ	6.8MΩ	6.2MΩ	6.8MΩ	6.2MΩ	6.8MΩ	6.2MΩ	6.8MΩ
code 0	7V	7.5V	63V	69V	Vin - .55	Vin - 0.12	19V	21V
code1	7.5V	8.5V	105V	115V	Vin - 1.35V	Vin - 1V	37V	41V
code2	8.5V	9.5V	152V	167V	Vin - 1.65V	Vin - 1.3V	55V	61V
code3	9.5V	10.5V	185V	203V	Vin - 2.5V	Vin - 2.2V	75V	82V
code4	11.5V	12.5V						
code5	12.5V	14V						
code6	17V	18.5V						
code7	21.5V	23.5V						

Table 8: SL2002 Fault Trigger Level Settings for Cres Voltage

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Startup Fault Condition Examples

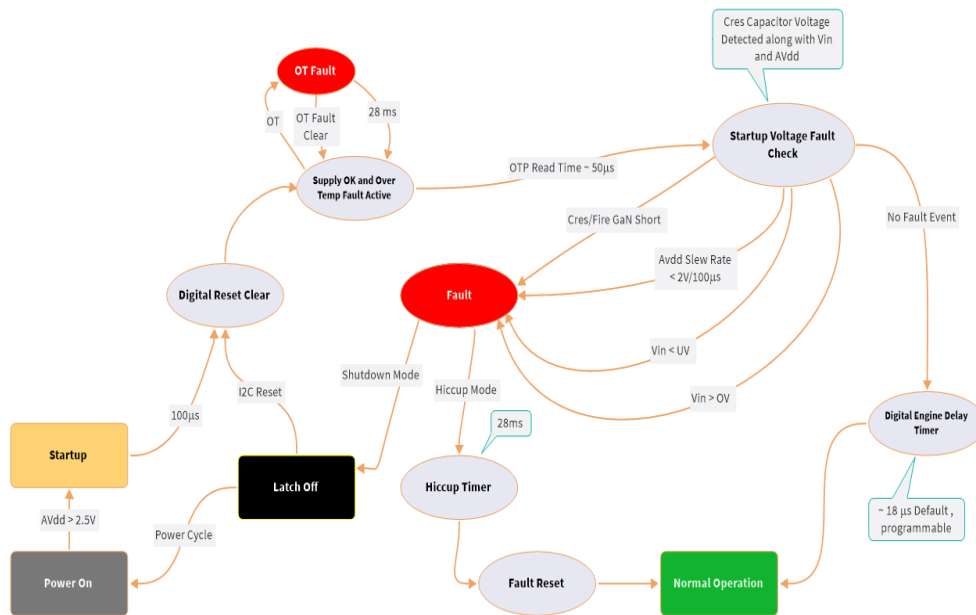


Figure 26: SL2002 Basic Startup Sequence

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I²C and Reg Map

Regmap

Key

read/write	The bit can be read/written from/to.
read only or write only	This bit can be read only. Writes have no effect.
read clear	Reading a 1 causes this bit to clear. Reading a 0 causes no action.
write clear	Writing a 1 causes this bit to clear. Writing a 0 causes no action.
one-hot	Writing a 1 causes a one-hot action. It will auto clear.

Name	Addr	B7	B6	B5	B4	B3	B2	B1	B0
Flux Time Control	0x10	FluxTime[7]	FluxTime[6]	FluxTime[5]	FluxTime[4]	FluxTime[3]	FluxTime[2]	FluxTime[1]	FluxTime[0]
Charge Time Cntrl	0x11	ChargeTime[7]	ChargeTime[6]	ChargeTime[5]	ChargeTime[4]	ChargeTime[3]	ChargeTime[2]	ChargeTime[1]	ChargeTime[0]
Fire Time Control	0x12	FireTime[7]	FireTime[6]	FireTime[5]	FireTime[4]	FireTime[3]	FireTime[2]	FireTime[1]	FireTime[0]
Function 3	0x13	SupplyOK_VTH[1]	SupplyOK_VTH[0]	VinOV_VTH[2]	VinOV_VTH[1]	VinOV_VTH[0]	DO NOT USE	VinUV_VTH[1]	VinUV_VTH[0]
Function 4	0x14	DutyCycleMode	FluxOV_VTH[1]	FluxOV_VTH[0]	FireOV_VTH[2]	FireOV_VTH[1]	FireOV_VTH[0]	FluxUV_VTH[1]	FluxUV_VTH[0]
Function 5	0x15	DigSoftRset	TChargeRef	TFireRef	TFluxRef[1]	TFluxRef[0]	TCharge2x	TFire2x	TFlux2x
Function 6	0x16	FluxOVBehavior[1]	FluxOVBehavior[0]	CresUVBehavior	FireUV_VTH[1]	FireUV_VTH[0]	DontSkip1stFlux	i2c_address[1]	i2c_address[0]
nvm_ctrl	0x8A	vpp_mode	test_mode[2:0]			vpp_req	wr_en	wr	rd
nvm_addr	0x8B	nvm_addr[7:0]							
nvm_wdata	0x8C	nvm_wdata[7:0]							
nvm_rdata	0x8D	nvm_rdata[7:0]							
status_fault	0x90	status_fault[7:4]				status_fault[3:0]			

Table 9: Register Map

OTP Read Delays

During start-up, Stingray will begin reading in the OTP ~100us after AVdd has reached a voltage of ~2.5V. The read-in of the OTP will take ~50us, at which time the CresSNS_UV Precharge comparator will be valid in order to detect a short from the cathode of the laser to ground. In order for this start-up short detection to trip immediately during start-up (before the laser light causes an eye safety concern), the VIN voltage should not rise to a voltage higher than the laser light threshold until at least 200us after the AVdd voltage is higher than 2.5V.

After OTP ready, the part will wait a programmable amount of time before the FluxOUT and FireOUT signals are enabled (allowed to go high), according to *Table 10: Fuse Time delay Programmability* below

bit5	bit4	Register 0x00, bits 5:4, FuseTime
0	0	Delay time from OTP read complete to Function mode allow is 20us
0	1	Delay time from OTP read complete to Function mode allow is 100us
1	0	Delay time from OTP read complete to Function mode allow is 400us
1	1	Delay time from OTP read complete to Function mode allow is 1000us

Table 10: Fuse Time delay Programmability

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Reference Design

A reference design for the evaluation board using SL2002 is shown below.

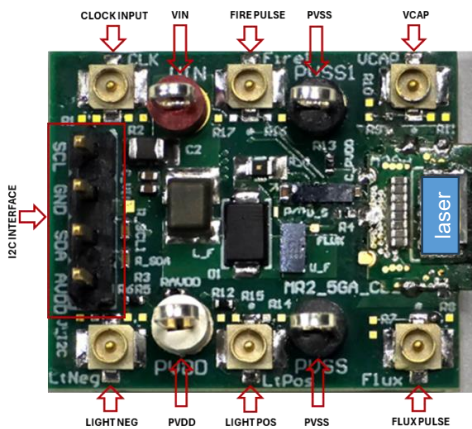
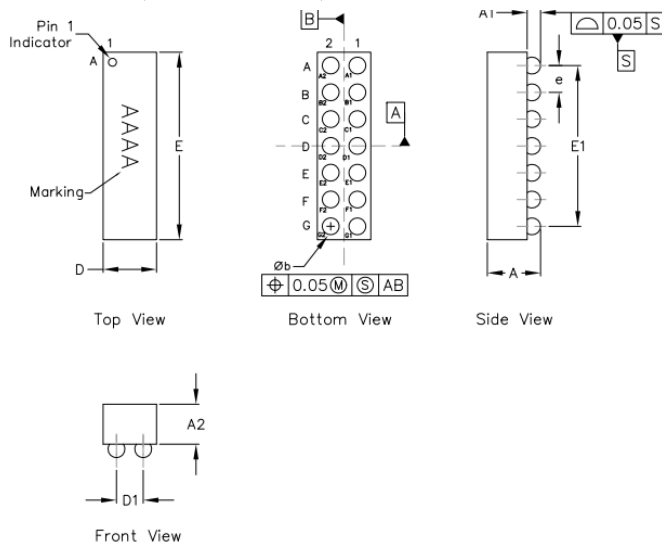


Figure 27:Evaluation Board

Package Dimensions



COMMON DIMENSION	
SYMBOL	VALUE
A	0.995 ±0.05
A1	0.250 ±0.03
A2	0.745 REF
b	ø 0.315 ±0.03
D	1.000 ±0.025
E	3.500 ±0.025
D1	0.50 BASIC
E1	2.50 BASIC
e	0.50 BASIC

- NOTE:
1. TERMINAL PITCH IS DEFINE BY THE TERMINAL CENTER TO CENTER.
 2. OUTER DIMENSION IS DEFINED BY CENTER LINES BETWEEN SCRIBE LINES
 3. ALL DIMENSIONS IN MILLIMETER
 4. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY
 5. TOLERANCE IS ±0.02 UNLESS SPECIFIED OTHERWISE

Commented [KB11]: Package profile and dimension TBD

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Figure 28: Package Dimensions

Product Ordering Information ^{Note 1}

Part Number	Package	Feature	Shipping Method
SL2002-00	14 Pin bumped flip chip		

Revision History

Revision	Date	Author	Note
1.0	3/25/2024	KB	Initial Release

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